Claims

[c1] An integrated circuit (IC) comprising:
a plurality of memory cells coupled in series to form a first memory group, wherein a memory cell comprises a capacitor coupled to a cell transistor;
a bitline coupled to a first end of the group; and
a first section switch is coupled to a second end of the group and a plateline, the section switch, when activated, selectively couples the plateline to the group.

[c2] The integrated circuit of claim 1 wherein the first section switch is activated to couple the group to the plateline when the group is selected and deactivated to decouple the plateline from the group when the group is not selected.

[c3] The integrated circuit of claim 1 further comprises:
a second memory group having a first end coupled to the bitline; and
a second section switch coupled to a second end of the second memory group and the plateline, the second section switch selectively coupling the second memory group to the plateline.

[c4] The integrated circuit of claim 3 wherein:
the first section switch is activated to couple the first memory group to the plateline when the memory group is selected and deactivated to decouple the plateline from the memory group when the memory group is not selected; and
the second section switch is activated to couple the second group to the plateline when the second group is selected and deactivated to decouple the plateline from the second group when the second group is not selected.

[c5] The integrated circuit of claim 3 wherein the first group is part of a first section of a memory array and the second group is part of a second section of the memory array.

[c6] The integrated circuit of claim 5 wherein:
the first section switch is activated to couple the first memory group to the plateline when the memory group is selected and deactivated to decouple the plateline from the memory group when the memory group is not selected; and

the second section switch is activated to couple the second group to the plateline when the second group is selected and deactivated to decouple the plateline from the second group when the second group is not selected.

[c7] The integrated circuit of claim 3 further comprises:
a complement bitline;
a first complement memory group having its first end coupled to the complement bitline;
a first complement section switch coupled to the plateline and a second end of the first complement memory group, the first complement section switch selectively coupling the first complement memory group to the plateline;
a second complement memory group having its first end coupled to the complement bitline; and
a second complement section switch coupled to the plateline and a second end of the first complement memory group, the first complement section switch selectively coupling the first complement memory group to the plateline.

[c8] The integrated circuit of claim 7 wherein the first section switch and first complement section switch are controlled by a first section selection signal and the second section switch and second complement section switch are controlled by a second section selection signal.

[c9] The integrated circuit of claim 7 wherein the first memory group and first complement memory group are part of a first section of a memory array and the second memory group and second complement memory group are part of a second section of the memory array.

[c10] The integrated circuit of claim 9 wherein the first complement section switch is activated to couple the first complement memory group to the plateline when the first complement memory group is selected and deactivated to decouple the plateline from the first complement memory group when the first complement memory group is not selected.

[c11] The integrated circuit of claim 3 further comprises:
a complement bitline;

a first complement memory group having its first end coupled to the complement bitline;

a first complement section switch coupled to a complement plateline and a second end of the first complement memory group, the first complement section switch selectively coupling the first complement memory group to the complement plateline;

a second complement memory group having its first end coupled to the complement bitline; and

a second complement section switch coupled to the complement plateline and a second end of the first complement memory group, the first complement section switch selectively coupling the first complement memory group to the complement plateline.

[c12] The integrated circuit of claim 11 wherein the first section switch and first complement switch are controlled by a first section selection signal and the second section switch and second complement section switch are controlled by a second selection signal.

[c13] The integrated circuit of claim 11 wherein the first memory group and first complement memory group are part of a first section of a memory array and the second memory group and second complement memory group are part of a second section of the memory array.

[c14] The integrated circuit of claim 13 wherein the first complement section switch is activated to couple the first complement memory group to the plateline when the first complement memory group is selected and deactivated to decouple the plateline from the first complement memory group when the first complement memory group is not selected.